

2/3-Phase PWM Controller for High-Density Power Supply

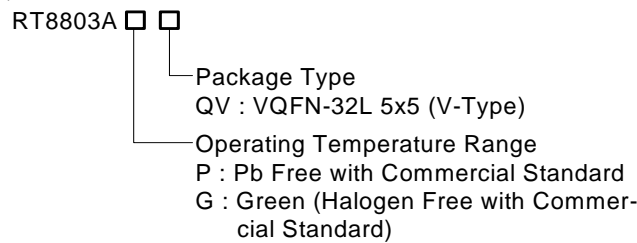
General Description

The RT8803A is a 2/3-phase synchronous buck controller specifically designed to power Intel®/AMD next generation microprocessors. It implements an internal 8-bit DAC that is identified by VID code of microprocessor directly. RT8803A generates VID table that conform to Intel® VRD10.x and VRD11 core power with 6.25mV increments and 0.5% accuracy.

RT8803A adopts innovative time-sharing DCR current sensing technique to sense phase currents for phase current balance, load line setting and over current protection. Using a common GM to sense all phase currents eliminates offset and linearity variation between GMs in conventional current sensing methods. As sub-milli-ohm-grade inductors are widely used in modern motherboards, slight offset and linearity mismatch will cause considerable current shift between phases. This technique ensures good current balance at mass production.

Other features include over current protection, programmable soft start, over voltage protection, and output offset setting. RT8803A comes to a small footprint package with VQFN-32L 5x5.

Ordering Information



Note :

Richtek Pb-free and Green products are :

- ▶RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶Suitable for use in SnPb or Pb-free soldering processes.
- ▶100% matte tin (Sn) plating.

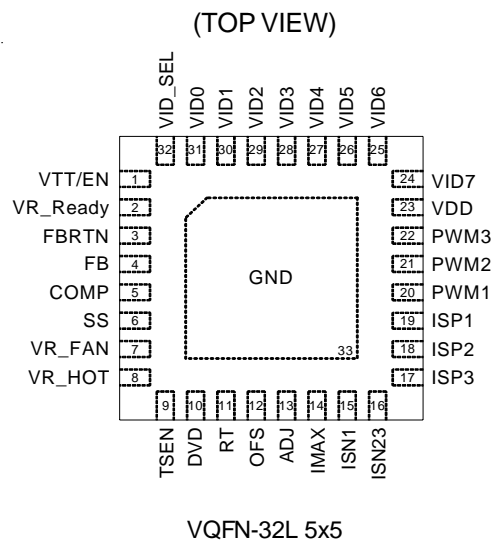
Features

- 5V Power Supply
- 2/3-Phase Power Conversion with Automatic Phase Selection
- 8-bit VID Interface, Supporting Intel VRD11/VRD10.x and AMD K8, K8_M2 CPUs
- VR_HOT and VR_FAN Indication
- Precision Core Voltage Regulation
- Power Stage Thermal Balance by DCR Current Sensing
- Adjustable Soft-start
- Over-Voltage Protection
- Adjustable Frequency and Typical at 300kHz per Phase
- Power Good Indication
- 32-Lead VQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

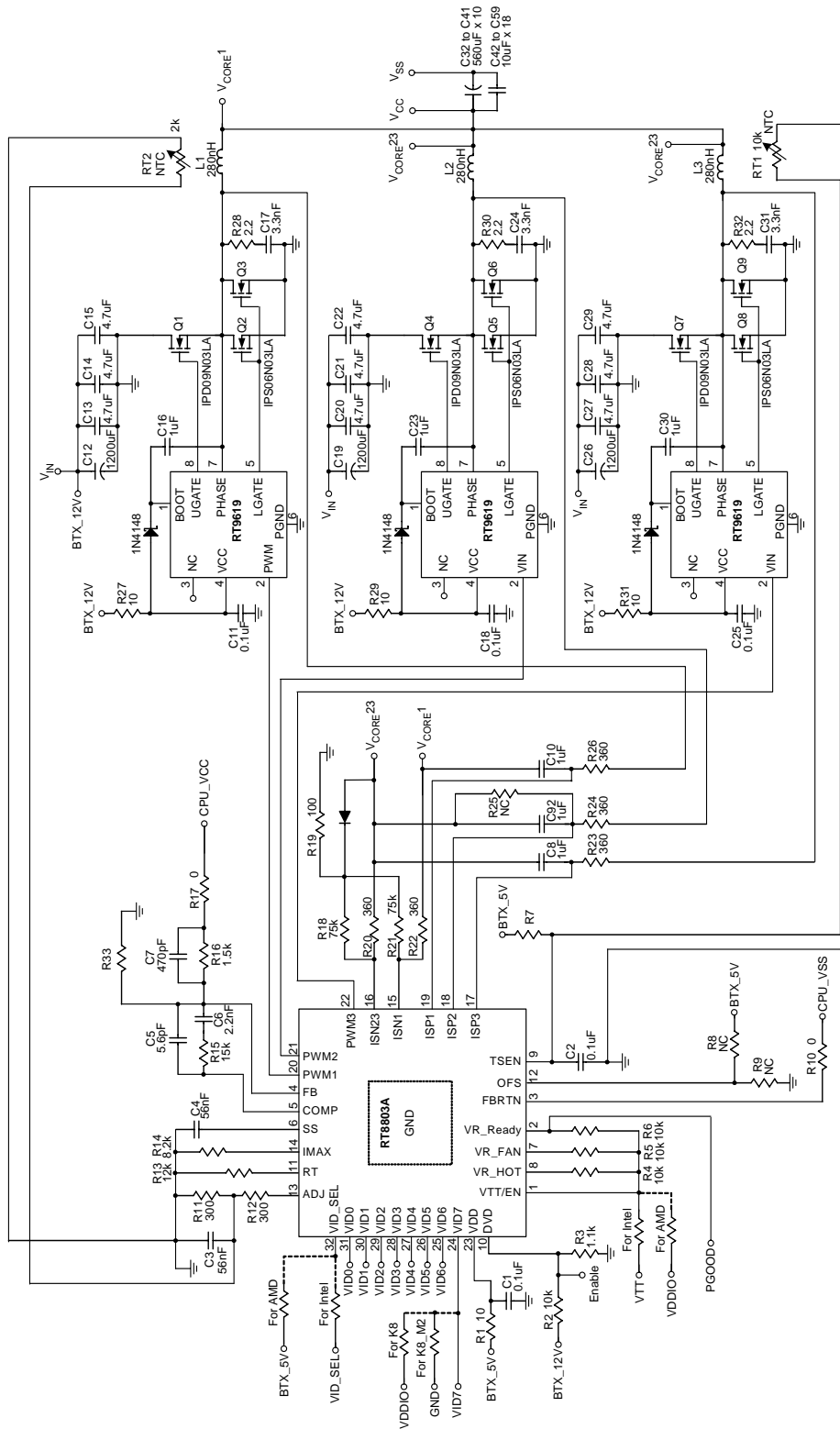
Applications

- Intel®/AMD New generation microprocessor for Desktop PC and Motherboard
- Low Output Voltage, High power density DC-DC Converters
- Voltage Regulator Modules

Pin Configurations



Typical Application Circuit



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Functional Pin Description

VTT/EN (Pin 1)

The pin is defined as the chip enable, and the VTT is applied for internal VID pull high power and power sequence monitoring.

VR_Ready (Pin 2)

Power good open-drain output.

FBRTN (Pin 3)

Feedback return pin. VIDDAC and error amplifier reference for remote sensing of the output voltage.

FB (Pin 4)

Inverting input pin of the internal error amplifier.

COMP (Pin 5)

Output pin of the error amplifier and input pin of the PWM comparator.

SS (Pin 6)

Connect this SS pin to GND with a capacitor to set the soft-start time interval.

VR_FAN (Pin 7)

The pin is defined to signal VR thermal information for external VR thermal dissipation scheme triggering.

VR_HOT (Pin 8)

The pin is defined to signal VR thermal information for external VR thermal dissipation scheme triggering.

TSEN (Pin 9)

Temperature detect pin for VR_HOT and VR_FAN.

DVD (Pin 10)

Programmable power UVLO detection input. Trip threshold is 1V at V_{DVD} rising.

RT (Pin 11)

The pin is defined to set internal switching operation frequency. Connect this pin to GND with a resistor R_{RT} to set the frequency F_{SW}.

$$F_{SW} = \frac{4.463 \text{ e}^9}{R_{RT} + 3500}$$

OFS (Pin 12)

The pin is defined for load line offset setting.

ADJ (Pin 13)

Current sense output for active droop adjusting. Connect a resistor from this pin to GND to set the load droop.

IMAX (Pin 14)

The pin is defined to set threshold of over current.

ISN1 (Pin 15)

Current sense negative input pin for channel 1 current sensing.

ISN23 (Pin 16)

Current sense negative input pins for channel 2 and channel 4 current sensing.

ISP1 (Pin 19), ISP2 (Pin 18), ISP3 (Pin 17)

Current sense positive input pins for individual converter channel current sensing.

PWM1 (Pin 20), PWM2 (Pin 21), PWM3 (Pin 22)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which using 2/3/4 channels, pull PWM 3/4/5 pins up to high.

VDD (Pin 23)

IC power supply. Connect this pin to a 5V supply.

VID7 (Pin 24), VID6 (Pin 25), VID5 (Pin 26), VID4 (Pin 27), VID3 (Pin 28), VID2 (Pin 29), VID1 (Pin 30), VID0 (Pin 31), VID_SEL (32)

DAC voltage identification inputs for VRD10.x / VRD11 / K8 / K8_M2 . These pins are internally pulled up to VTT.

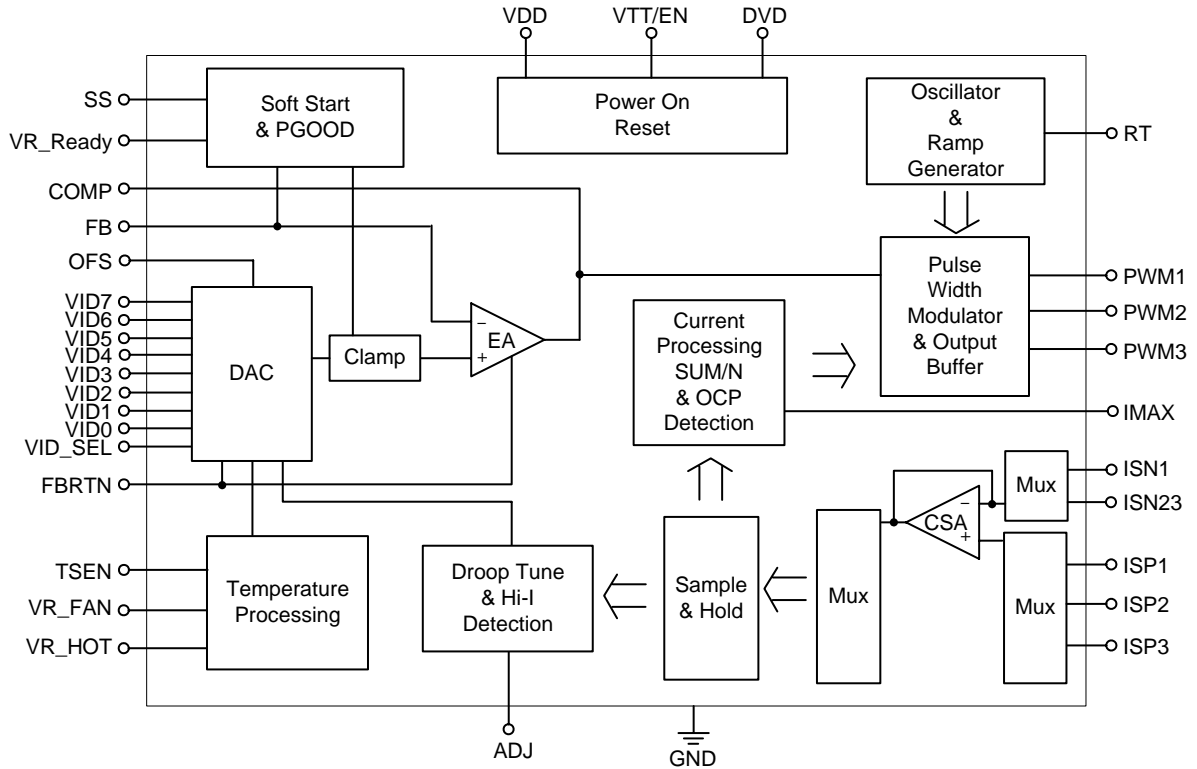
| VIDSEL | VID [7] | Table |
|--------|---------|--------|
| VTT | X | VR11 |
| GND | X | VR10.x |
| VDD | NC | K8 |
| VDD | GND | K8_M2 |

GND [Exposed pad (33)]

The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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Function Block Diagram



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Table 1. Output Voltage Program (VRD10.x + VID6)

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1.60000V |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1.59375V |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.58750V |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1.58125V |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1.57500V |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1.56875V |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1.56250V |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1.55625V |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1.55000V |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1.54375V |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1.53750V |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1.53125V |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1.52500V |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1.51875V |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1.51250V |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1.50625V |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1.50000V |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1.49375V |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1.48750V |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1.48125V |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1.47500V |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1.46875V |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1.46250V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1.45625V |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1.45000V |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1.44375V |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1.43750V |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1.43125V |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1.42500V |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1.41875V |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1.41250V |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1.40625V |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1.40000V |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1.39375V |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1.38750V |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1.38125V |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1.37500V |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1.36875V |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1.36250V |

To be continued

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Table 1. Output Voltage Program (VRD10.x + VID6)

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1.35625V |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1.35000V |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1.34375V |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1.33750V |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1.33125V |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1.32500V |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1.31875V |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1.31250V |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1.30625V |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1.30000V |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1.29375V |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1.28750V |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1.28125V |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1.27500V |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1.26875V |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1.26250V |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1.25625V |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1.25000V |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1.24375V |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1.23750V |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1.23125V |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1.22500V |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1.21875V |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1.21250V |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1.20625V |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1.20000V |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1.19375V |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1.18750V |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1.18125V |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1.17500V |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1.16875V |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1.16250V |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1.15625V |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1.15000V |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1.14375V |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1.13750V |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1.13125V |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1.12500V |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1.11875V |

To be continued

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Table 1. Output Voltage Program (VRD10.x + VID6)

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1.11250V |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1.10625V |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1.10000V |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1.09375V |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | OFF |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.08750V |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.08125V |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.07500V |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.06875V |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.06250V |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.05625V |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.05000V |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.04375V |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.03750V |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.03125V |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.02500V |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.01875V |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.01250V |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.00625V |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.00000V |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0.99375V |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0.98750V |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0.98125V |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0.97500V |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0.96875V |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0.96250V |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0.95625V |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0.95000V |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0.94375V |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0.93750V |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0.93125V |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0.92500V |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0.91875V |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0.91250V |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0.90625V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0.90000V |

To be continued

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Table 1. Output Voltage Program (VRD10.x + VID6)

| Pin Name | | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|------|-------------------------------|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | VID6 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0.89375V |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0.88750V |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0.88125V |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0.87500V |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0.86875V |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0.86250V |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0.85625V |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0.85000V |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0.84375V |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.83750V |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0.83125V |

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Table 2. Output Voltage Program (VRD11)

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| 00 | OFF |
| 01 | OFF |
| 02 | 1.60000V |
| 03 | 1.59375V |
| 04 | 1.58750V |
| 05 | 1.58125V |
| 06 | 1.57500V |
| 07 | 1.56875V |
| 08 | 1.56250V |
| 09 | 1.55625V |
| 0A | 1.55000V |
| 0B | 1.54375V |
| 0C | 1.53750V |
| 0D | 1.53125V |
| 0E | 1.52500V |
| 0F | 1.51875V |
| 10 | 1.51250V |
| 11 | 1.50625V |
| 12 | 1.50000V |
| 13 | 1.49375V |
| 14 | 1.48750V |
| 15 | 1.48125V |
| 16 | 1.47500V |
| 17 | 1.46875V |
| 18 | 1.46250V |
| 19 | 1.45625V |
| 1A | 1.45000V |
| 1B | 1.44375V |
| 1C | 1.43750V |
| 1D | 1.43125V |
| 1E | 1.42500V |
| 1F | 1.41875V |
| 20 | 1.41250V |
| 21 | 1.40625V |
| 22 | 1.40000V |
| 23 | 1.39375V |
| 24 | 1.38750V |
| 25 | 1.38125V |
| 26 | 1.37500V |

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| 27 | 1.36875V |
| 28 | 1.36250V |
| 29 | 1.35625V |
| 2A | 1.35000V |
| 2B | 1.34375V |
| 2C | 1.33750V |
| 2D | 1.33125V |
| 2E | 1.32500V |
| 2F | 1.31875V |
| 30 | 1.31250V |
| 31 | 1.30625V |
| 32 | 1.30000V |
| 33 | 1.29375V |
| 34 | 1.28750V |
| 35 | 1.28125V |
| 36 | 1.27500V |
| 37 | 1.26875V |
| 38 | 1.26250V |
| 39 | 1.25625V |
| 3A | 1.25000V |
| 3B | 1.24375V |
| 3C | 1.23750V |
| 3D | 1.23125V |
| 3E | 1.22500V |
| 3F | 1.21875V |
| 40 | 1.21250V |
| 41 | 1.20625V |
| 42 | 1.20000V |
| 43 | 1.19375V |
| 44 | 1.18750V |
| 45 | 1.18125V |
| 46 | 1.17500V |
| 47 | 1.16875V |
| 48 | 1.16250V |
| 49 | 1.15625V |
| 4A | 1.15000V |
| 4B | 1.14375V |
| 4C | 1.13750V |
| 4D | 1.13125V |

To be continued

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Table 2. Output Voltage Program (VRD11)

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| 4E | 1.12500V |
| 4F | 1.11875V |
| 50 | 1.11250V |
| 51 | 1.10625V |
| 52 | 1.10000V |
| 53 | 1.09375V |
| 54 | 1.08750V |
| 55 | 1.08125V |
| 56 | 1.07500V |
| 57 | 1.06875V |
| 58 | 1.06250V |
| 59 | 1.05625V |
| 5A | 1.05000V |
| 5B | 1.04375V |
| 5C | 1.03750V |
| 5D | 1.03125V |
| 5E | 1.02500V |
| 5F | 1.01875V |
| 60 | 1.01250V |
| 61 | 1.00625V |
| 62 | 1.00000V |
| 63 | 0.99375V |
| 64 | 0.98750V |
| 65 | 0.98125V |
| 66 | 0.97500V |
| 67 | 0.96875V |
| 68 | 0.96250V |
| 69 | 0.95625V |
| 6A | 0.95000V |
| 6B | 0.94375V |
| 6C | 0.93750V |
| 6D | 0.93125V |
| 6E | 0.92500V |
| 6F | 0.91875V |
| 70 | 0.91250V |
| 71 | 0.90625V |
| 72 | 0.90000V |
| 73 | 0.89375V |
| 74 | 0.88750V |

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| 75 | 0.88125V |
| 76 | 0.87500V |
| 77 | 0.86875V |
| 78 | 0.86250V |
| 79 | 0.85625V |
| 7A | 0.85000V |
| 7B | 0.84375V |
| 7C | 0.83750V |
| 7D | 0.83125V |
| 7E | 0.82500V |
| 7F | 0.81875V |
| 80 | 0.81250V |
| 81 | 0.80625V |
| 82 | 0.80000V |
| 83 | 0.79375V |
| 84 | 0.78750V |
| 85 | 0.78125V |
| 86 | 0.77500V |
| 87 | 0.76875V |
| 88 | 0.76250V |
| 89 | 0.75625V |
| 8A | 0.75000V |
| 8B | 0.74375V |
| 8C | 0.73750V |
| 8D | 0.73125V |
| 8E | 0.72500V |
| 8F | 0.71875V |
| 90 | 0.71250V |
| 91 | 0.70625V |
| 92 | 0.70000V |
| 93 | 0.69375V |
| 94 | 0.68750V |
| 95 | 0.68125V |
| 96 | 0.67500V |
| 97 | 0.66875V |
| 98 | 0.66250V |
| 99 | 0.65625V |
| 9A | 0.65000V |
| 9B | 0.64375V |

To be continued

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Table 2. Output Voltage Program (VRD11)

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| 9C | 0.63750V |
| 9D | 0.63125V |
| 9E | 0.62500V |
| 9F | 0.61875V |
| A0 | 0.61250V |
| A1 | 0.60625V |
| A2 | 0.60000V |
| A3 | 0.59375V |
| A4 | 0.58750V |
| A5 | 0.58125V |
| A6 | 0.57500V |
| A7 | 0.56875V |
| A8 | 0.56250V |
| A9 | 0.55625V |
| AA | 0.55000V |
| AB | 0.54375V |
| AC | 0.53750V |
| AD | 0.53125V |
| AE | 0.52500V |
| AF | 0.51875V |
| B0 | 0.51250V |
| B1 | 0.50625V |
| B2 | 0.50000V |
| B3 | X |
| B4 | X |
| B5 | X |
| B6 | X |
| B7 | X |
| B8 | X |
| B9 | X |
| BA | X |
| BB | X |
| BC | X |
| BD | X |
| BE | X |
| BF | X |
| C0 | X |
| C1 | X |
| C2 | X |

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| C3 | X |
| C4 | X |
| C5 | X |
| C6 | X |
| C7 | X |
| C8 | X |
| C9 | X |
| CA | X |
| CB | X |
| CC | X |
| CD | X |
| CE | X |
| CF | X |
| D0 | X |
| D1 | X |
| D2 | X |
| D3 | X |
| D4 | X |
| D5 | X |
| D6 | X |
| D7 | X |
| D8 | X |
| D9 | X |
| DA | X |
| DB | X |
| DC | X |
| DD | X |
| DE | X |
| DF | X |
| E0 | X |
| E1 | X |
| E2 | X |
| E3 | X |
| E4 | X |
| E5 | X |
| E6 | X |
| E7 | X |
| E8 | X |
| E9 | X |

To be continued

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Table 2. Output Voltage Program (VRD11)

| Pin Name | Nominal Output Voltage DACOUT |
|----------|-------------------------------|
| HEX | |
| EA | X |
| EB | X |
| EC | X |
| ED | X |
| EE | X |
| EF | X |
| F0 | X |
| F1 | X |
| F2 | X |
| F3 | X |
| F4 | X |
| F5 | X |
| F6 | X |
| F7 | X |
| F8 | X |
| F9 | X |
| FA | X |
| FB | X |
| FC | X |
| FD | X |
| FE | OFF |
| FF | OFF |

Note: (1) 0 : Connected to GND

(2) 1 : Open

(3) X : Don't Care

Table 3. Output Voltage Program (K8)

| VID4 | VID3 | VID2 | VID1 | VID0 | Nominal Output Voltage DACOUT |
|------|------|------|------|------|-------------------------------|
| 0 | 0 | 0 | 0 | 0 | 1.550 |
| 0 | 0 | 0 | 0 | 1 | 1.525 |
| 0 | 0 | 0 | 1 | 0 | 1.500 |
| 0 | 0 | 0 | 1 | 1 | 1.475 |
| 0 | 0 | 1 | 0 | 0 | 1.450 |
| 0 | 0 | 1 | 0 | 1 | 1.425 |
| 0 | 0 | 1 | 1 | 0 | 1.400 |
| 0 | 0 | 1 | 1 | 1 | 1.375 |
| 0 | 1 | 0 | 0 | 0 | 1.350 |
| 0 | 1 | 0 | 0 | 1 | 1.325 |
| 0 | 1 | 0 | 1 | 0 | 1.200 |
| 0 | 1 | 0 | 1 | 1 | 1.275 |
| 0 | 1 | 1 | 0 | 0 | 1.250 |
| 0 | 1 | 1 | 0 | 1 | 1.225 |
| 0 | 1 | 1 | 1 | 0 | 1.200 |
| 0 | 1 | 1 | 1 | 1 | 1.175 |
| 1 | 0 | 0 | 0 | 0 | 1.150 |
| 1 | 0 | 0 | 0 | 1 | 1.125 |
| 1 | 0 | 0 | 1 | 0 | 1.100 |
| 1 | 0 | 0 | 1 | 1 | 1.075 |
| 1 | 0 | 1 | 0 | 0 | 1.050 |
| 1 | 0 | 1 | 0 | 1 | 1.025 |
| 1 | 0 | 1 | 1 | 0 | 1.000 |
| 1 | 0 | 1 | 1 | 1 | 0.975 |
| 1 | 1 | 0 | 0 | 0 | 0.950 |
| 1 | 1 | 0 | 0 | 1 | 0.925 |
| 1 | 1 | 0 | 1 | 0 | 0.900 |
| 1 | 1 | 0 | 1 | 1 | 0.875 |
| 1 | 1 | 1 | 0 | 0 | 0.850 |
| 1 | 1 | 1 | 0 | 1 | 0.825 |
| 1 | 1 | 1 | 1 | 0 | 0.800 |
| 1 | 1 | 1 | 1 | 1 | Shutdown |

Note: (1) 0 : Connected to GND
 (2) 1 : Open

Table 4. Output Voltage Program (K8_M2)

| Pin Name | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|-------------------------------|
| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.5500 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.5250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.4750 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.4250 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.3750 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.3500 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.3250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.2750 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.2250 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.1750 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.1500 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.1250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.0750 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.0250 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.9750 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.9500 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.9250 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.8750 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.8250 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.7750 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.7500 |

To be continued

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Table 4. Output Voltage Program (K8_M2)

| Pin Name | | | | | | Nominal Output Voltage DACOUT |
|----------|------|------|------|------|------|-------------------------------|
| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.7250 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.6875 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.6750 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.6625 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.6500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.6375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.6250 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.6125 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.6000 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.5875 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.5750 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5625 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.5500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.5375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.5250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.5125 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.5000 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.4875 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.4750 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.4625 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.4500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.4375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.4250 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.4125 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.3875 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.3750 |

Note: (1) 0 : Connected to GND

(2) 1 : Open

(3) The voltage above are load independent for desktop and server platforms. For mobile platforms the voltage above correspond to zero load current.

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ----- 7V
- Input, Output or I/O Voltage ----- GND-0.3V to $V_{DD}+0.3V$
- Power Dissipation, P_D @ $T_A = 25^\circ C$
 VQFN-32L 5x5 ----- 2.778W
- Package Thermal Resistance (Note 4)
 VQFN-32L 5x5, θ_{JA} ----- 36°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 2)
 HBM (Human Body Mode) ----- 2kV
 MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{DD} ----- $5V \pm 10\%$
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{DD} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|--------------------|------------------|-----------------------|------|------|------|-------|
| V_{DD} Supply Current | | | | | | | |
| Nominal Supply Current | | I_{DD} | PWM 1,2,3 Open | -- | 12 | 16 | mA |
| Power-On Reset | | | | | | | |
| POR Threshold | | V_{DDRTH} | V_{DD} Rising | 4.0 | 4.2 | 4.5 | V |
| Hysteresis | | V_{DDHYS} | | 0.2 | 0.5 | -- | V |
| V_{DVD} Threshold | Trip (Low to High) | V_{DVDTH} | Enable | 0.9 | 1.0 | 1.1 | V |
| | Hysteresis | V_{DVDHYS} | | -- | 60 | -- | mV |
| V_{TT} Threshold | Trip (Low to High) | V_{TTTH} | Enable | 0.75 | 0.85 | 0.95 | V |
| | Hysteresis | V_{TTHYS} | | -- | 0.1 | -- | |
| Oscillator | | | | | | | |
| Free Running Frequency | | f_{OSC} | $R_{RT} = 20k\Omega$ | 180 | 200 | 220 | kHz |
| Frequency Adjustable Range | | f_{OSC_ADJ} | | 50 | -- | 400 | kHz |
| Ramp Amplitude | | ΔV_{OSC} | $R_{RT} = 20k\Omega$ | -- | 1.9 | -- | V |
| Ramp Valley | | V_{RV} | | 0.7 | 1.0 | -- | V |
| Maximum On-Time of Each Channel | | | Three Phase Operation | 62 | 67 | 72 | % |
| RT Pin Voltage | | V_{RT} | $R_{RT} = 20k\Omega$ | 0.9 | 1.0 | 1.1 | V |

To be continued

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|-----------------------------------|------------------|-----------------------------|-------------------|-----|-------------------|------------|
| Reference and DAC | | | | | | |
| DACOUT Voltage Accuracy | ΔV_{DAC} | $V_{DAC} \geq 1V$ | -0.5 | -- | +0.5 | % |
| | | $1V \geq V_{DAC} \geq 0.8V$ | -5 | -- | +5 | mV |
| | | $V_{DAC} < 0.8V$ | -8 | -- | +8 | mV |
| DAC (VID0-VID125) Input Low | V_{ILDAC} | | -- | -- | $1/2V_{TT} - 0.2$ | V |
| DAC (VID0-VID125) Input High | V_{IHDAC} | | $1/2V_{TT} + 0.2$ | -- | -- | V |
| V_{ID} Pull-up Resistance | | | 12 | 15 | 18 | k Ω |
| OFS Pin Voltage | V_{OFS} | $R_{OFS} = 100k\Omega$ | 0.9 | 1.0 | 1.1 | V |
| Error Amplifier | | | | | | |
| DC Gain | | | -- | 65 | -- | dB |
| Gain-Bandwidth Product | GBW | | -- | 10 | -- | MHz |
| Slew Rate | SR | COMP = 10pF | -- | 8 | -- | V/ μ s |
| Current Sense GM Amplifier | | | | | | |
| CSN Full Scale Source Current | I_{ISPFSS} | | 100 | -- | -- | μ A |
| CSN Current for OCP | | | 150 | -- | -- | μ A |
| Protection | | | | | | |
| Over-Voltage Trip (FB-DACOUT) | ΔOVT | | 100 | 150 | 200 | mV |
| IMAX Voltage | V_{IMAX} | $R_{IMAX} = 20k$ | 0.9 | 1.0 | 1.1 | V |
| Power Good | | | | | | |
| Output Low Voltage | V_{PGOODL} | $I_{PGOOD} = 4mA$ | -- | -- | 0.2 | V |

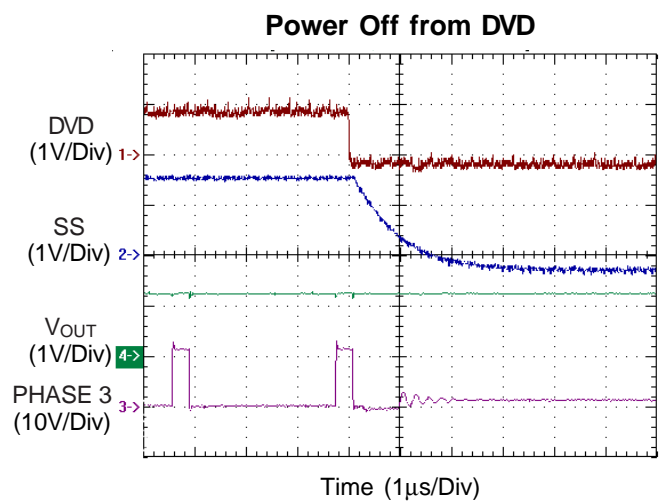
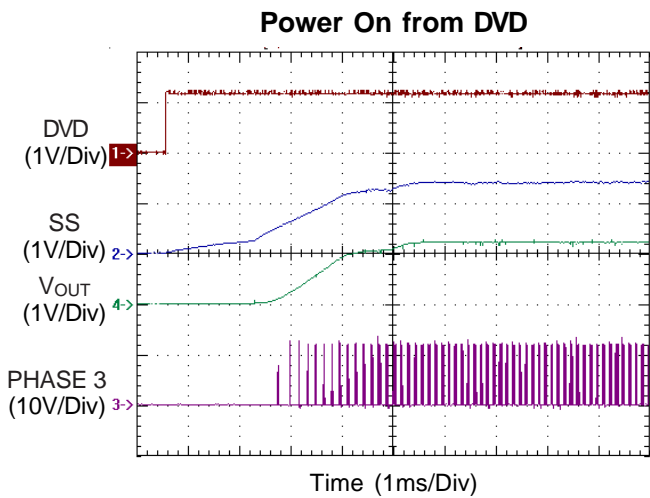
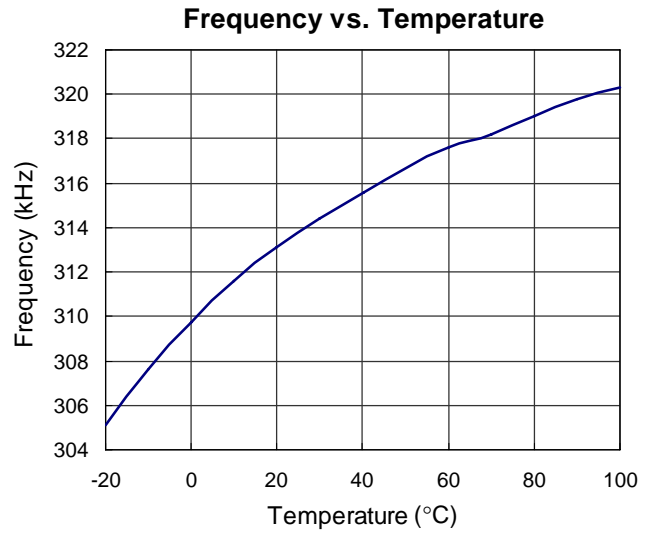
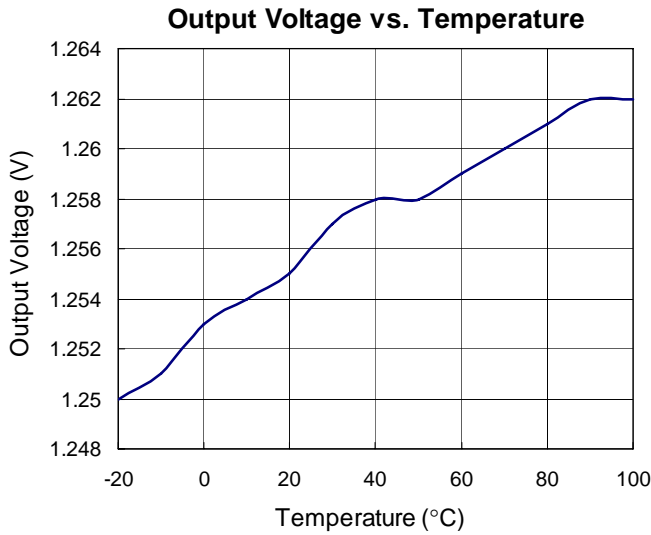
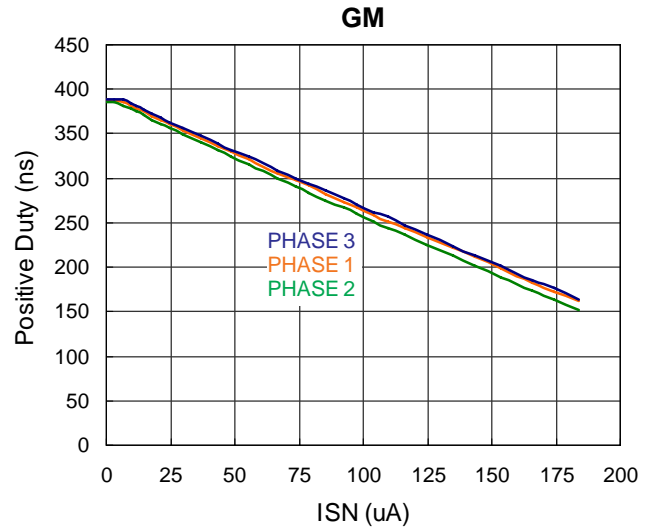
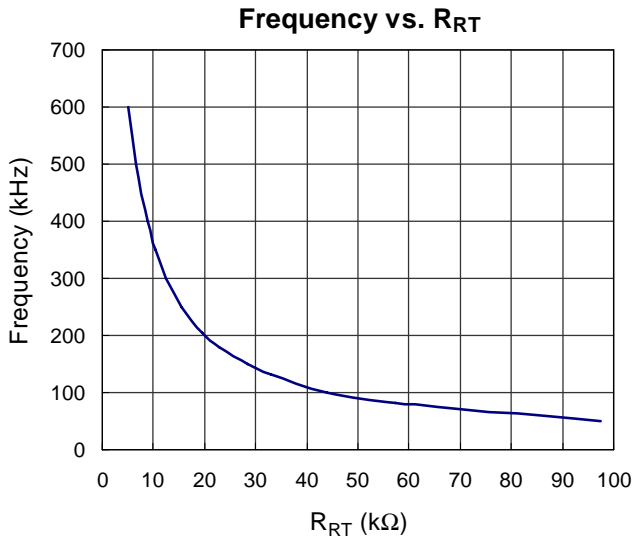
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

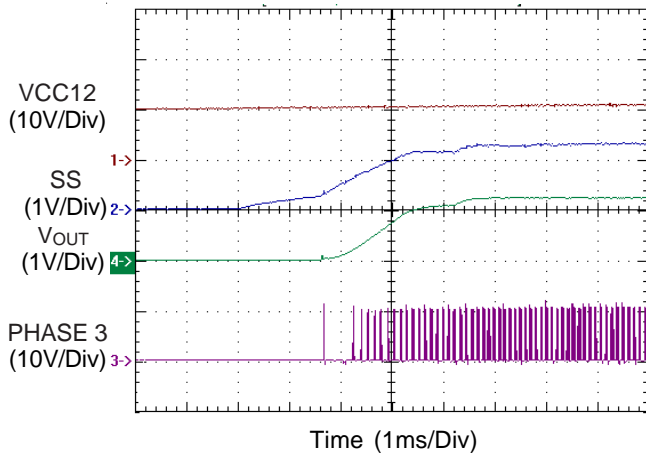
Note 4. θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

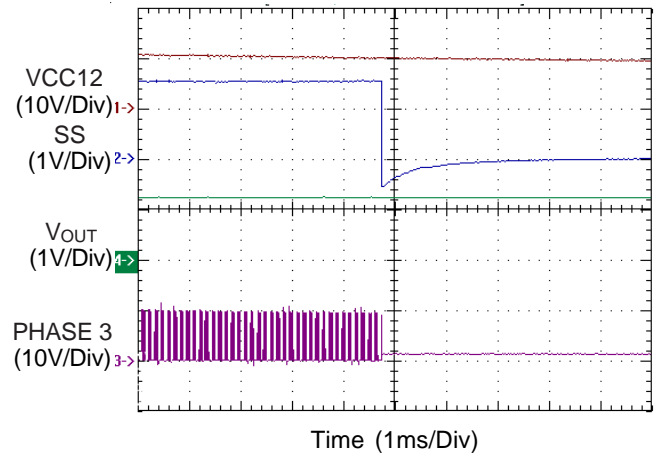


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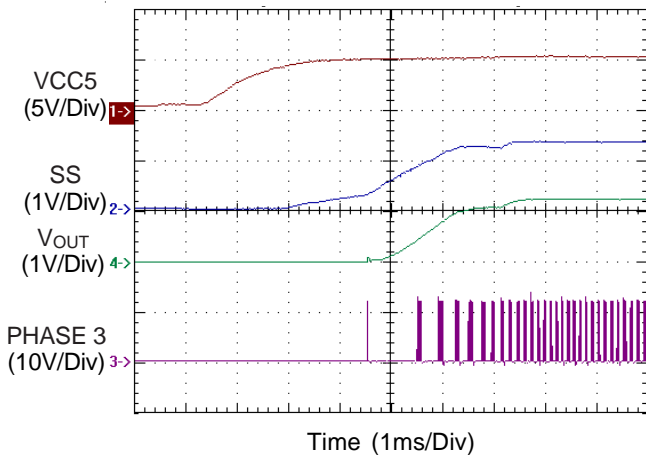
Power On from VCC12



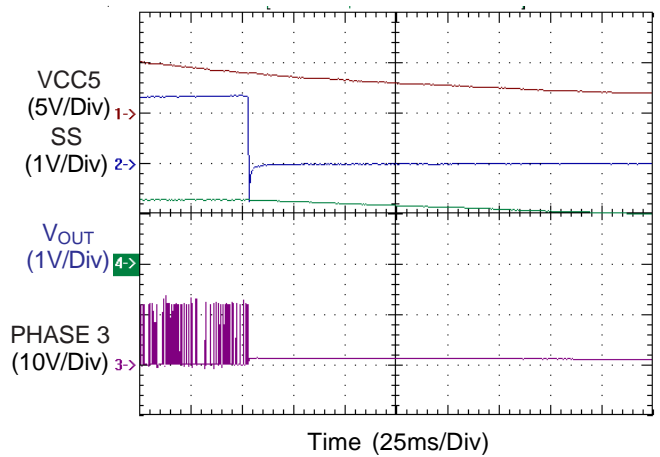
Power Off from VCC12



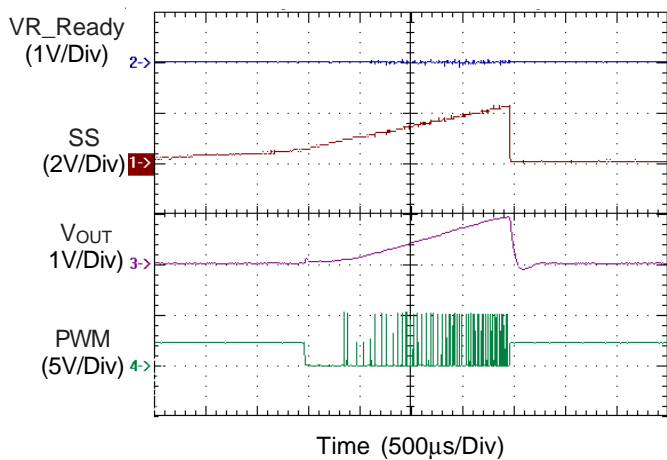
Power On from VCC5



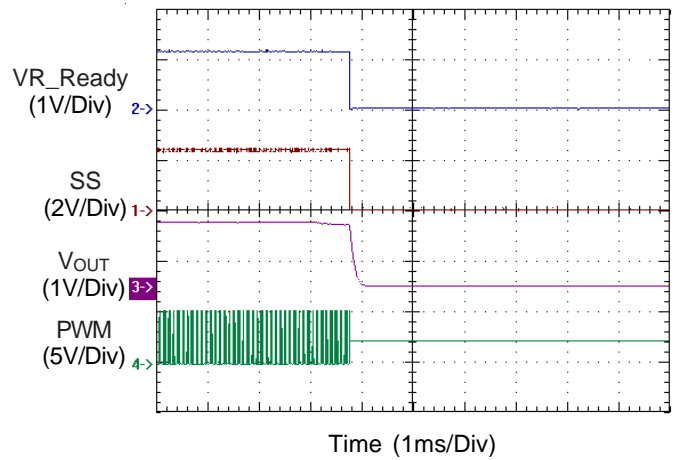
Power Off from VCC5



Power On with OCP

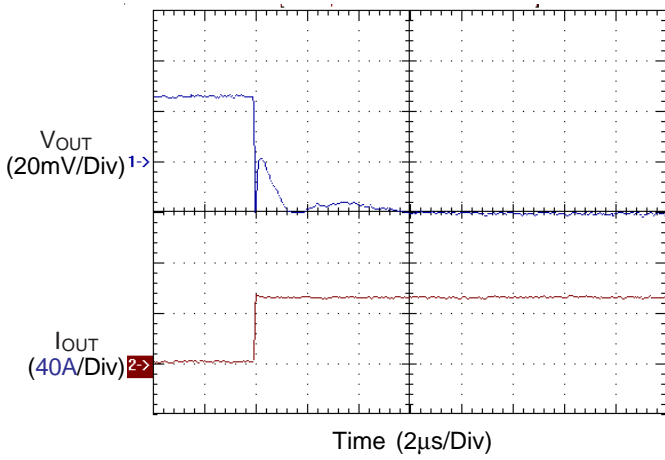


Output Short Circuit

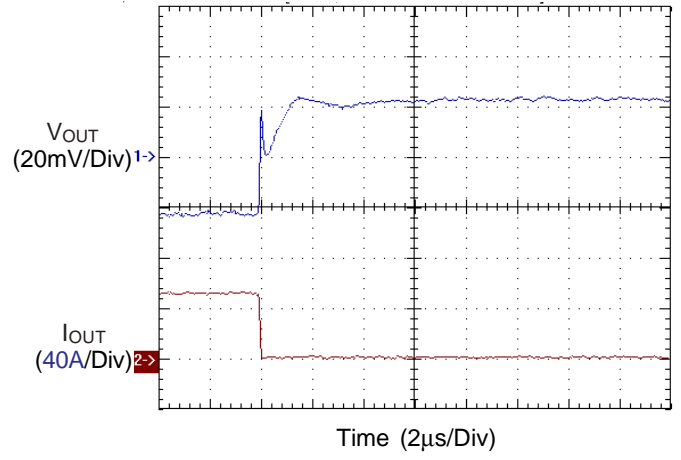


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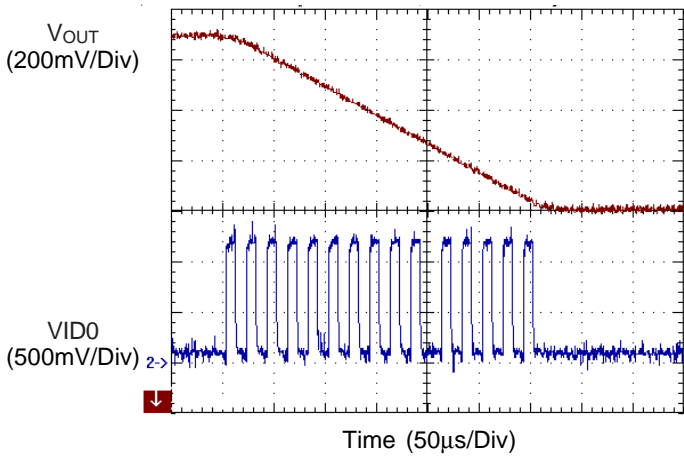
V_{OUT} Droop



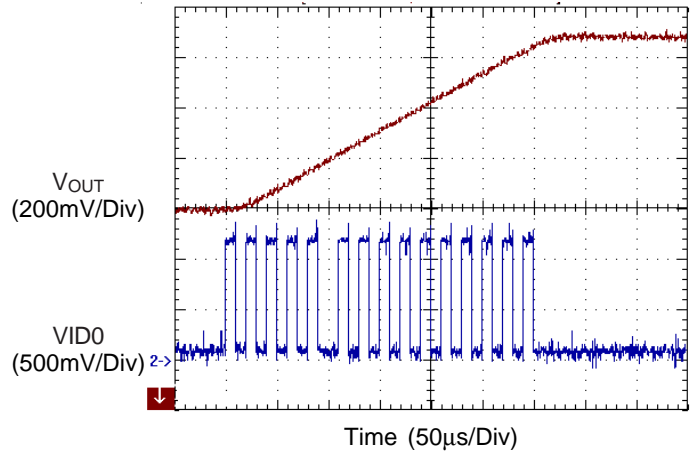
V_{OUT} Overshoot



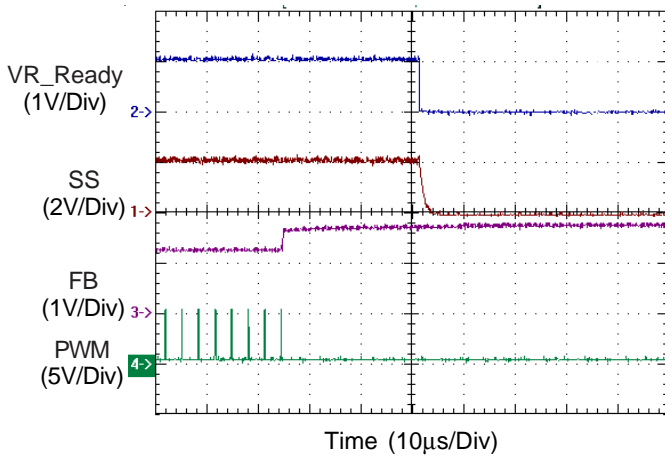
Dynamic VID



Dynamic VID



OVP



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Applications Information

RT8803A is a multi-phase DC/DC controller specifically designed to deliver high quality power for next generation CPU. RT8803A controls a special power-on sequence & monitors the thermal condition of VR module to meet the VRD11 requirement. Phase currents are sensed by innovative time-sharing DCR current sensing technique for channel current balance, droop tuning, and over current protection. Using one common GM amplifier for current sensing eliminates offset errors and linearity variation between GMs. As sub-milli-ohm-grade inductors are widely used in modern mother boards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time-sharing DCR current sensing technique is extremely important to guarantee phase current balance in mass production.

Converter Initialization, Phase Selection, and Power Good Function

The RT8803A initiates only after 3 pins are ready: VDD pin power on reset (POR), VTT/EN pin enabled, and DVD pin is higher than 1V. VDD POR is to make sure RT8803A is powered by a voltage for normal work. The rising threshold voltage of VDD POR is 4.2V typically. At VDD POR, RT8803A checks PWM3, PWM4 and PWM5 status to determine phase number of operation. Pull high PWM3 for two-phase operation; pull high PWM4 for three-phase operation; pull high PWM5 for four-phase operation. The unused current sense pins should be connected to GND or left floating.

VTT/EN acts as a chip enable pin and receives signal from FSB or other power management IC.

DVD is to make sure that ATX12V is ready for drivers to work normally. Connect a voltage divider from ATX12V to DVD pin as shown in the Typical Application Circuit. Make sure that DVD pin voltage is below its threshold voltage before drivers are ready and above its threshold voltage for minimum ATX12V during normal operation.

If any one of VDD, VTT/EN, and DVD is not ready, RT8803A keeps its PWM outputs high impedance and the companion drivers turn off both upper and lower MOSFETs. After VDD, VTT/EN, and DVD are ready, RT8803A initiates its soft start cycle that is compliant

with Intel®VRD11 specification as shown in Figure 1. A time-variant internal current source charges the capacitor connected to SS pin. SS voltage ramps up piecewise linearly and locks VID_DAC output with a specified voltage drop. Consequently, V_{CORE} is built up according to VID_DAC output and meet Intel® VRD11 requirement. VR_READY output is pulled high by external resistor when V_{CORE} reaches VID_DAC output with 1~2ms delay. An SS capacitor about 47nF is recommend for VRD11 compliance.

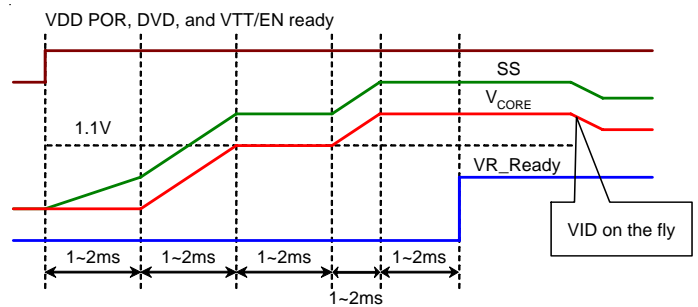


Figure 1. Timing Diagram During Soft Start Interval

Voltage Control

CPU V_{CORE} voltage is Kelvin sensed by FB and FBRTN pins and precisely regulated to VID_DAC output by internal high gain Error Amplifier (EA). The sensed signal is also used for power good and over voltage function. The typical OVP trip point is 170mV above VID_DAC output. RT8803A pulls PWM outputs low and latches up upon OVP trip to prevent damaging the CPU. It can only restart by resetting one of VDD, DVD, or VTT/EN pin.

RT8803A supports Intel VRD10.x, VRD11, AMD K8 and AMD K8_M2 VID specification.

The change of VID_DAC output at VID on the fly is also smoothed by capacitor connected to SS pin. Consequently, V_{core} shifts to its new position smoothly as shown in Figure 2.

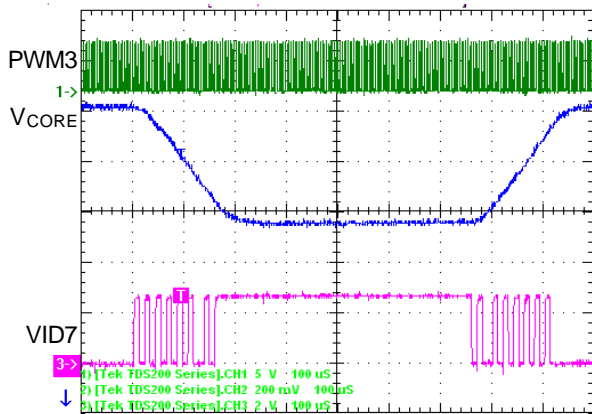


Figure 2. Vcore Response at VID on the Fly

DCR Current Sensing

RT8803A adopts an innovative time-sharing DCR current sensing technique to sense the phase currents for phase current balance (phase thermal balance) and load line regulation as shown in Figure 3. Current sensing amplifier GM samples and holds voltages VCx across the current sensing capacitor Cx by turns in a switching cycle. According to the Basic Circuit Theory, if

$$\frac{I_x}{DCR_x} = R_x \times C_x \text{ then } VC_x = I_{LX} \times DCR_x$$

Consequently, the sensing current I_x is proportional to inductor current I_{LX} and is expressed as :

$$I_x = \frac{I_{LX} \times DCR_x}{R_{CSNX}}$$

The sensed current I_x is used for current balance and droop tuning as described as followed. Since all phases share one common GM, GM offset and linearity variation effect is eliminated in practical applications. As sub-milli-ohm-grade inductors are widely used in modern mother boards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time-sharing DCR current sensing technical is extremely important to guarantee phase current balance in mass production.

Phase Current Balance

The sampled and held phase current I_x are summed and averaged to get the averaged current \bar{I}_x . Each phase current I_x then is compared with the averaged current. The difference between I_x and \bar{I}_x is injected to corresponding PWM comparator. If phase current I_x is smaller than the averaged current, RT8803A increases the duty cycle of corresponding phase to increase the phase current accordingly and vice versa.

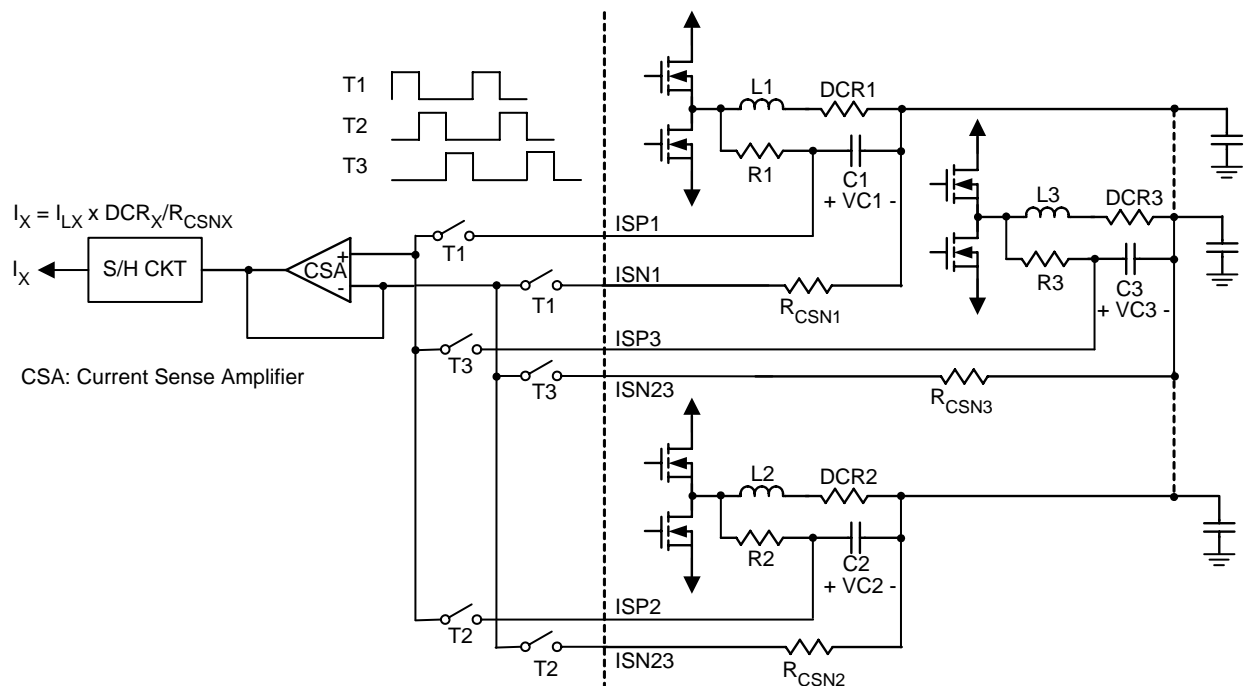


Figure 3

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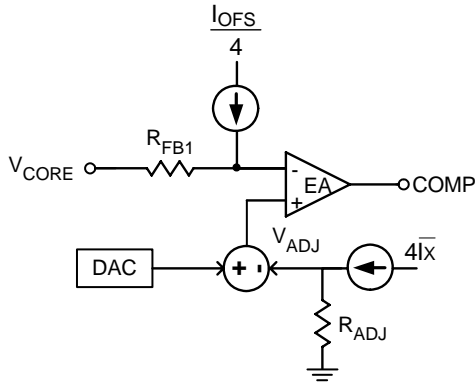


Figure 4. Load Line and Offset Function

Output Voltage Offset Function

To meet Intel® requirement of initial offset of load line, RT8803A provides programmable initial offset function. External resistor R_{OFS} and voltage source at OFS pin generate offset current $I_{OFS} = \frac{V_{OFS}}{R_{OFS}}$, where V_{OFS} is 1V typical. One quarter of I_{OFS} flows through R_{FB1} as shown in Figure 4. Error amplifier would hold the inverting pin equal to $V_{DAC} - V_{ADJ}$. Thus output voltage is subtracted from $V_{DAC} - V_{ADJ}$ for a constant offset voltage.

$$V_{CORE} = V_{DAC} - V_{ADJ} - \frac{R_{FB1}}{4 \times R_{OFS}}$$

A positive output voltage offset is possible by connecting R_{OFS} to VDD instead of to GND. Please note that when R_{OFS} is connected to VDD, V_{OFS} is $V_{DD} - 2V$ typically and half of I_{OFS} flows through R_{FB1} . V_{CORE} is rewritten as :

$$V_{CORE} = V_{DAC} - V_{ADJ} + \frac{R_{FB1}}{R_{OFS}}$$

Current Ratio Setting

Current ratio adjustment is possible as described below. It is important for achieving thermal balance in practical application where thermal conditions between phases are not identical. Figure 5 shows the application circuit of GM for current ratio requirement. According to Basic Circuit Theory

$$V_{Cx} = \frac{\frac{R_{PX}}{R_X + R_{PX}}}{\frac{S R_X \times R_{PX} \times C_X}{R_X + R_{PX}} + 1} \times I_{LX} \times DCRx$$

If $\frac{L_X}{DCRx} = (R_X // R_{PX}) \times C_x$ then

$$V_{Cx} = \frac{R_{PX}}{R_X + R_{PX}} \times I_{LX} \times DCRx$$

With other phase kept unchanged, this phase would share $(R_{PX} + R_X) / R_{PX}$ times current than other phases. Figure 6 and 7 show different current ratio setting for the power stage when Phase 3 is programmed 2 times current than other phases. Figure 8 and 9 compare the above current ratio setting results.

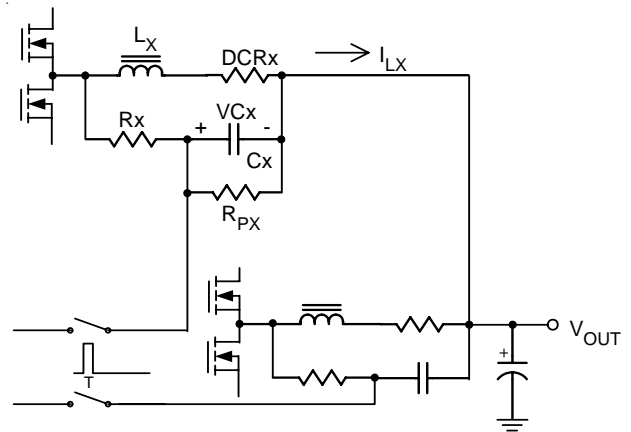


Figure 5

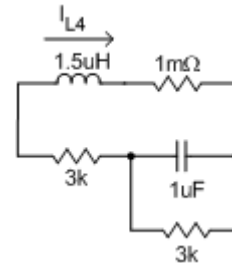


Figure 6. GM3 Setting for current ratio function

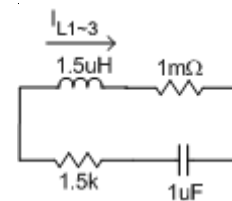


Figure 7. GM1~2 Setting for current ratio function

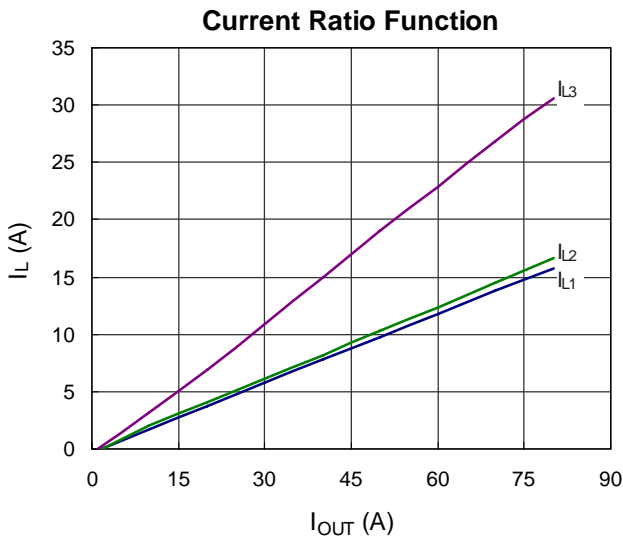


Figure 8

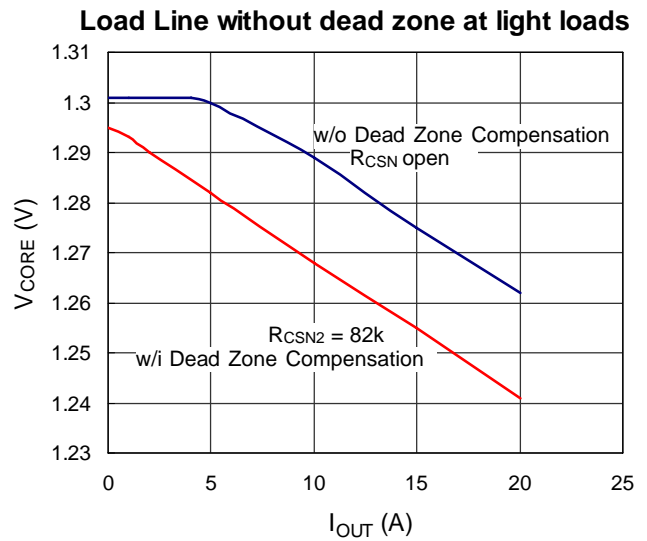


Figure 10

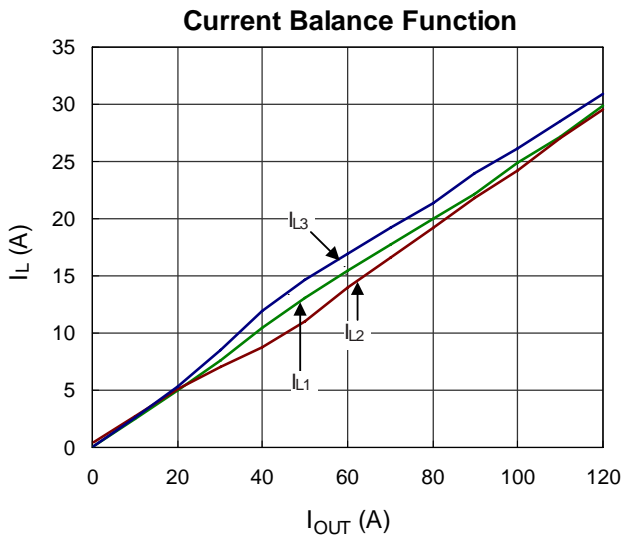


Figure 9

Dead Zone Elimination

RT8803A samples and holds inductor current at 50% period by time-sharing sourcing a current I_x to R_{CSN} . At light load condition when inductor current is not balance, voltage V_{Cx} across the sensing capacitor would be negative. It needs a negative I_x to sense the voltage. However, RT8803A CANNOT provide a negative I_x and consequently cannot sense negative inductor current. This results in dead zone of load line performance as shown in Figure 10. Therefore a technique as shown in Figure 11 is required to eliminate the dead zone of load line at light load condition.

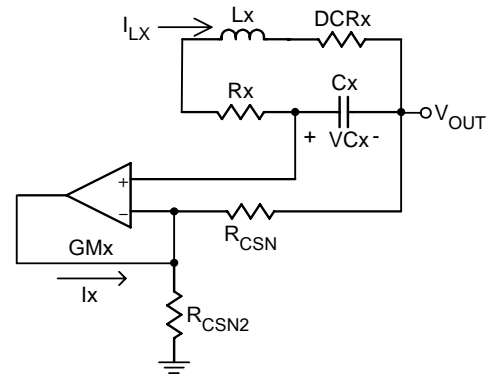


Figure 11. Application circuit of GM

Referring to Figure 11, I_x is expressed as :

$$I_x = \frac{V_{OUT}}{R_{CSN2}} + \frac{I_{Lx_66\%} \times DCR_x}{R_{CSN2}} + \frac{I_{Lx_66\%} \times DCR_x}{R_{CSN}} \quad (1)$$

where $I_{Lx_50\%}$ is the of inductor current at 50% period. To make sure RT8803A could sense the inductor current, right hand side of Equation (1) should always be positive:

$$\frac{V_{OUT}}{R_{CSN2}} + \frac{I_{Lx_66\%} \times DCR_x}{R_{CSN2}} + \frac{I_{Lx_66\%} \times DCR_x}{R_{CSN}} \geq 0 \quad (2)$$

Since $R_{CSN} \gg DCR_x$ in practical application, Equation (2) could be simplified as :

$$\frac{V_{OUT}}{R_{CSN2}} \geq \left| \frac{I_{Lx_66\%} \times DCR_x}{R_{CSN}} \right|$$

For example, assuming the negative inductor current is $I_{LX_50\%} = -5A$ at no load, then for

$$R_{CSN} = 330\Omega, R_{ADJ} = 160\Omega, V_{OUT} = 1.300V$$

$$\frac{1.3V}{R_{CSN2}} \geq \left| \frac{-5A \times 1m\Omega}{330\Omega} \right|$$

$$R_{CSN2} \leq 85.8k\Omega$$

Choose $R_{CSN2} = 82k\Omega$

Figure 10 shows that dead zone of load line at light load is eliminated by applying this technique.

VR_HOT & VR_FAN Setting

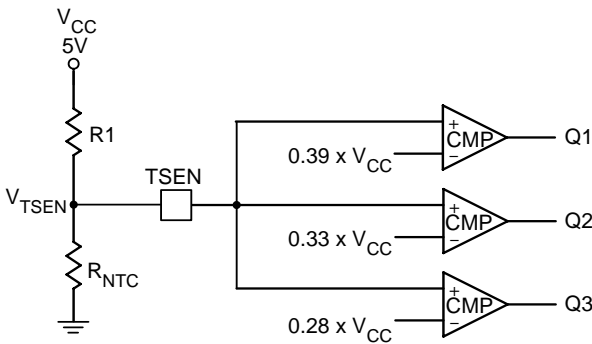


Figure 12

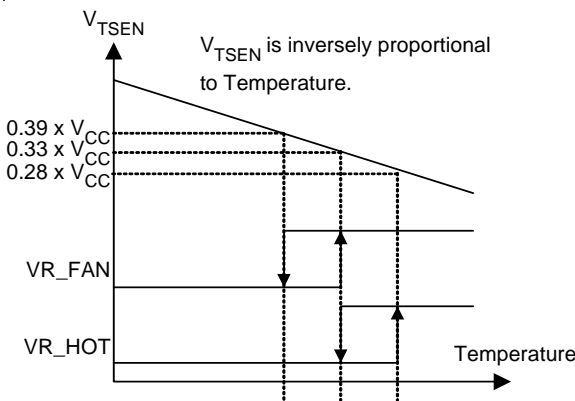


Figure 13. VR_HOT and VR_FAN Signal vs TSEN Voltage

Load Line Setting and Thermal Compensation

$$V_{ADJ} = \text{Sum}(I_x) \times R_{ADJ} = (DCR \times R_{ADJ} / R_{CSN}) \times I_{OUT}$$

$$= LL \times I_{OUT}$$

$$V_{OUT} = V_{DAC} - V_{ADJ} = V_{DAC} - LL \times I_{OUT}$$

$$LL = DCR(PTC) \times R_{ADJ}(NTC) / R_{CSN}$$

DCR is the inductor DCR which is a PTC resistance.

If R_{ADJ} is connected as in Figure 14, $R_{ADJ} = R1 + (R2 // R_{NTC})$, which is a negative temperature correlated resistance. By properly selecting R1 and R2, the positive temperature coefficient of DCR can be canceled by the negative temperature coefficient of R_{ADJ} . Thus the load line will be thermally compensated.

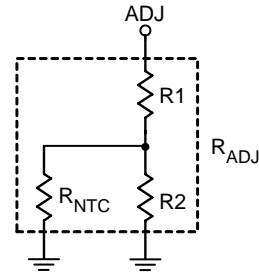


Figure 14. R_{ADJ} Connection for Thermal Compensation

Over Current Protection

Phase current OCP

RT8803A uses an external resistor R_{IMAX} connected to IMAX pin to generate a reference current I_{IMAX} for over current protection :

$$I_{IMAX} = \frac{V_{IMAX}}{R_{IMAX}}$$

where V_{IMAX} is typical 1.0V . OCP comparator compares each sensed phase current I_x with this reference current as shown in Figure 15. Equivalently, the maximum phase current $I_{LX(MAX)}$ is calculated as below:

$$\frac{1}{3} I_{X(MAX)} = \frac{1}{2} I_{IMAX}$$

$$I_{X(MAX)} = \frac{3}{2} I_{IMAX} = \frac{3}{2} \times \frac{V_{IMAX}}{R_{IMAX}}$$

$$I_{LX(MAX)} = I_x \times \frac{R_{CSNX}}{DCR_x} = \frac{3}{2} \times \frac{V_{IMAX}}{R_{IMAX}} \times \frac{R_{CSNX}}{R_{LX}}$$

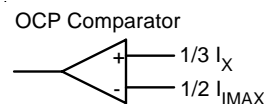


Figure 15. Over Current Comparator

Error Amplifier Characteristic

For fast response of converter to meet stringent output current transient response, RT8803A provides large slew rate capability and high gain-bandwidth performance.

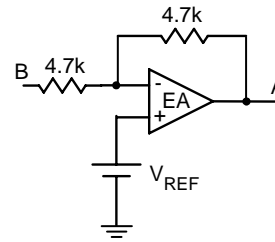


Figure 18. Gain-Bandwidth Measurement by signal A divided by signal B

EA Falling Slew Rate

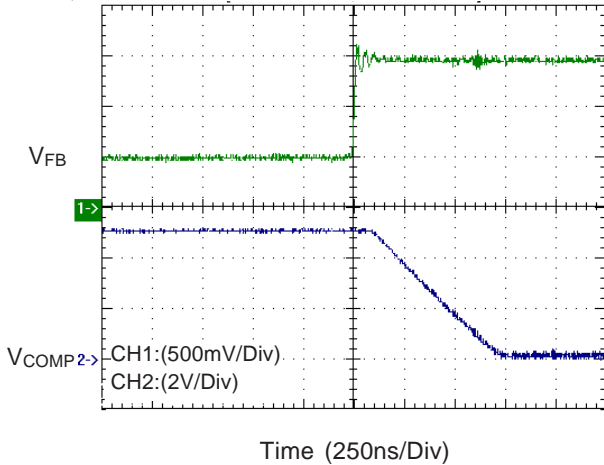


Figure 16. EA Rising Transient with 10pF Loading ; Slew Rate = 10V/μs

EA Rising Slew Rate

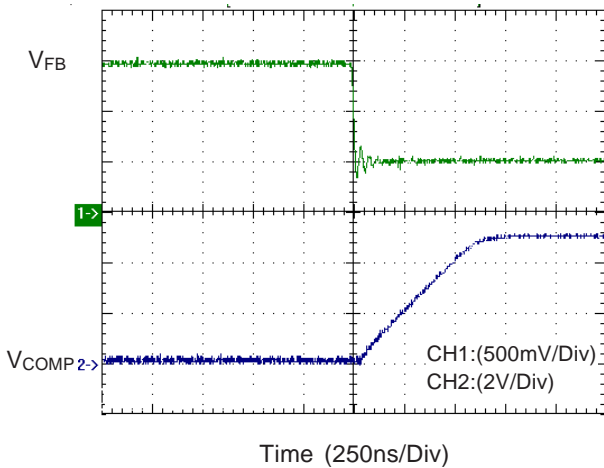


Figure 17. EA Falling Transient with 10pF Loading ; Slew Rate = 8V/μs

Design Procedure Suggestion

- Output filter pole and zero (Inductor, output capacitor value & ESR).
- Error amplifier compensation & saw-tooth wave amplitude (compensation network).
- Kelvin sense for V_{CORE} .

Current Loop Setting

- GM amplifier S/H current (current sense component DCR, ISP_X and ISN_X pin external resistor value).
- Over-current protection trip point (R_{IMAX} resistor).

VRM Load Line Setting

- Droop amplitude (ADJ pin resistor).
- No load offset (R_{CSN})
- DAC offset voltage setting (OFS pin & compensation network resistor).
- Temperature coefficient compensation (TSEN external resistor & thermistor, resistor between ADJ and GND.)

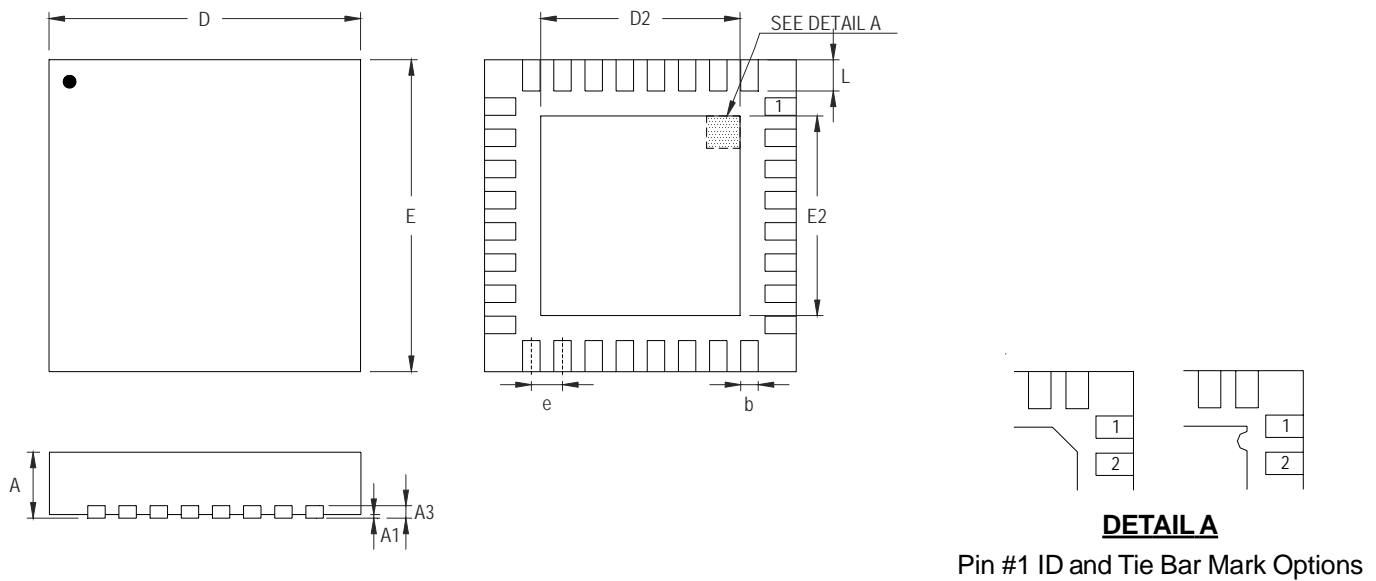
Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

- Kelvin sense for current sense GM amplifier input.
- Refer to layout guide for other items.

Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 4.950 | 5.050 | 0.195 | 0.199 |
| D2 | 3.400 | 3.750 | 0.134 | 0.148 |
| E | 4.950 | 5.050 | 0.195 | 0.199 |
| E2 | 3.400 | 3.750 | 0.134 | 0.148 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

V-Type 32L QFN 5x5 Package

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